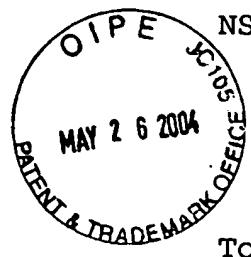


*ZFW*



NSI-03-001

May 21, 2004

To: Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/796,386 03/09/04 |

Jun Ho Cho et al.

OUTPUT BUFFER WITH CONTROLLED  
SLEW RATE FOR DRIVING A RANGE  
OF CAPACITIVE LOADS

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
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P.O. Box 1450, Alexandria, VA 22313-1450, on May 24, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

*S.B.A.* 5/24/04

U.S. Patent 5,926,651 to Johnston et al., "Output Buffer with Current Paths Having Different Current Carrying Characteristics for Providing Programmable Slew Rate and Signal Strength," describes a method where an output buffer slew rate is controlled by providing logic signals to the buffer circuit that switch in or out drive transistors with different current capability.

U.S. Patent 5,808,478 to Andresen, "Digitally Controlled Output Buffer to Incrementally Match Line Impedance and Maintain Slew Rate Independent of Capacitive Output Loading," discloses a method where the output buffer slew rate is varied by comparing the output voltage transition time against a reference.

U.S. Patent 6,265,913 to Lee et al., "Load Driving Circuits Having Adjustable Output Drive Capability," teaches a method where the output buffer fall time is controlled by comparing the load capacitance against a threshold capacitance.

U.S. Patent 6,583,644 to Shin, "Output Buffer for Reducing Slew Rate Variation," describes a method where slew rate is controlled by comparison of input data rise time against bias voltages which vary with processing.

R. Senthinathan et al., "Application Specific CMOS Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise," IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, Dec. 1993, pp. 1383-1388, describes an output driver where turn on of pull-up and pull-down output transistors are sequenced to control slew rate and avoid switching noise.

Sincerely,



Stephen B. Ackerman,  
Reg. No. 37761

